

Circuit comprising mutually asynchronous circuit modules

Systems on silicon show a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions. This is enabled by the increasing density with which components can be integrated on an integrated circuit. At the same time the clock speed at which circuits are operated tends to increase too. The higher clock speed in combination with the increased density of components has reduced the area which can operate synchronously within the same clock domain. This has created the need for a modular approach. According to such an approach the processing system comprises a plurality of relatively independent circuit modules operating mutually asynchronously. Internally these modules may be driven synchronously by a local clock, or may operate asynchronously.

In a particular case the asynchronous modules are peripherals which are coupled via a bus to a main module, for example via a bridge. Communication between two mutually asynchronous circuit modules can be done via either clock bridging buffers (for data streams) or clock bridging variables. Examples of clock bridging variables are so-called command and status registers in the interface between a processor bus and peripheral units.

It is an object of the invention to provide a circuit supporting a consistent and efficient data transfer between mutually asynchronous circuit modules. According to the invention this object is achieved by

A circuit comprising a first and a second circuit module and a synchronization module, the first and the second module being mutually a-synchronous, and being coupled by the synchronization module, the synchronization module comprising

- a transfer register for storing data which is communicated between the two circuit modules,
- a control circuit for generating a control signal for the transfer register in response to a respective timing signal from the first and the second circuit module, the control circuit comprising at least
 - a repeater for inducing changes in the value of the control signal,

- at least one edge sensitive element for delaying active edges in the control signal until a synchronizing transition in a selected one of the timing signals is detected,

5 In the circuit of the invention data to be communicated is stored in the transfer register. The control circuit achieves that when the transfer register is being updated both circuit modules are not involved in either changing write data (WDAT) or using read data (RDAT).

10 Therefore, the data being transferred is always consistent, and with a small delay and few minor interruptions always available to the module reading the data. The control chain may be extended with portions of the first and the second circuit module.

These and other aspects are described in more detail with reference to the drawing. Therein

15 Figure 1 schematically shows a circuit according to the invention.

Figure 2 shows in more detail an embodiment of the synchronization module.

Figure 2A shows a detail in a particular embodiment of this embodiment.

Figure 3 shows a further embodiment of the synchronization module.

Figure 4 shows again a further embodiment of the synchronization module.

20 Figure 5 shows a still further embodiment of the synchronization module.

In these Figures elements having reference numbers which differ by 100 or a multiple thereof have the same or a similar function.

25 Figure 1 schematically shows a circuit according to the invention. It comprises a first circuit module 10, a second circuit module 20, which are mutually asynchronous, and a synchronization module 30.

30 The synchronization module 30 comprises a transfer register 31 for temporarily storing data which is transferred from the first 10 to the second circuit module 20 and a transfer register 33 for storing data that is communicated in the opposite direction. The transfer registers 31 and 33 are controlled by a control circuit 32 which operates in response to respective timing signal St1, St2 from the first and the second circuit module 10,20.

Timing signal St1 may have a regular nature, such as a clock signal or may be irregular, the synchronization transitions in that signal indicate that its write data (WDAT0) will be stable

for a longer period after a short delay and that its ingoing read data signal (RDAT1) will not be used for a longer period. In this case the first circuit module 10 is a clocked module with clock signal St1 and the second module 20 is an asynchronous module with handshake signals St2 and St3. St2 is used by circuit module 20 to request access to the transfer registers 5 and St3 is an acknowledge signal by which the synchronization module 30 indicates the right to access the registers. The control circuit 32 comprises a control chain for generating a control signal CR that controls the registers 31 and 33. The control circuit 32 includes a repeater 34 for inducing transitions in the value of the control signal CR, and at least one edge sensitive element 35 for delaying an active transition in the control signal value until a 10 synchronization transition in a selected one of the timing signals (here the signal St1) is detected. In addition the control chain comprises an arbitration element 38. The first and the second circuit module may be integrated on a chip, or may be part of different chips. The circuit may include one or more further circuit modules.

The circuit shown in Figure 1 operates as follows. The control chain generates 15 signal CR which is used to control the transfer registers in 3 stages. The repeater 34 amends the value of control signal CR1, for example by inversion, to obtain the second stage CR2. An active transition in signal CR2 is delayed until a synchronization transition is detected in timing signal St1 by the edge sensitive element 35. The synchronized control signal CR3 is one of the inputs of an arbiter (38), which has request signal St2 as the other input. The 20 arbiter blocks active transitions in CR3 when circuit module 20 has the right to access the transfer registers. When circuit module 20 is not using the transfer registers, the active transitions in signal CR3 are passed on to signal CR4.

This event enables the transfer registers to store their input values: WDAT0 in register 31 and WDAT1 in register 33. By means of timing signal St2 the second circuit 25 module 20 indicates that it wants to communicate: read RDAT0 or change WDAT1 (or both). Timing signal St3 indicates to module 20 that it has the right to read RDAT0 and change WDAT1. The arbitrator 38 then blocks active transitions in signal CR, so that the transfer registers do not change their value until circuit module 20 indicates via signal St2 that it has completed the communication

30 For the control signals one can use two- or four-phase signaling. In a two-phase signaling scheme all transitions are active. In a four-phase signaling scheme either the rising or the falling edges are active. The preferred embodiment of the invention is four-phase handshake signaling with the rising edges as active transitions. In that case the edge sensitive element 35 has to delay both transitions until it is triggered by the timing signal St1.

Practical implementations for the elements used in the present invention such as wait elements, edge sensitive elements, arbiters, sequencers and repeaters are well known to the person skilled in the art of asynchronous signal processing, and will therefore not be described in detail here.

5 Figure 2 shows in more detail an embodiment of the synchronization module 30. Parts therein corresponding to those of Fig. 1 have a reference number, which is 100 higher. The module shown therein further comprises a comparator 136 for generating a difference signal ΔD upon detection of a difference between an input and an output of the transfer register 131. The control chain further comprises a wait element 137 for delaying an
10 active transition in the control signal CR until a difference is detected between the input and the output of the transfer register. The circuit shown in Figure 2 comprises a first circuit module 110 which provides a clock signal Wclk as the selected timing signal. The timing signal from the second circuit module 120 is a read request signal Rreq. The arbiter 138 has its first channel being arranged between an output of the edge sensitive element 135 and an
15 input of the repeater 134. Its second channel has a first input for receiving the read request signal Rreq and a second output for providing a read acknowledge signal Rack to the second circuit module.

The operation of the circuit shown in Figure 2 differs from the circuit shown in Figure 1 in the following respect. If no new data is offered to the transfer register 131, i.e. if
20 the data offered at the input of transfer register 131 is equal to the data stored therein, the control signal AD is false, and consequently the wait element 137 blocks the active transitions in the control signal. As the wait element 137 forms a closed chain with the elements 134, 135 and 138 all activity in the chain is suspended until new data is offered to the transfer register 131. This measure may reduce the power consumption of the circuit.

25 Alternatively the synchronization module 130 may have a register 133 for temporarily storing data WDAT1 from the second circuit module 120 to provide this as data RDAT1 to the first circuit module 110 instead of the register 131. Additionally the synchronization module 130 may have a comparator 136' for comparing the data WDAT1 and RDAT1 to control the wait element 137. Alternatively the synchronization circuit may
30 both comprise a register 131 for temporarily storing WDAT0 and a register 133 for storing WDAT1 as is shown in Figure 2A. Likewise the synchronization module may have a comparator 136' for comparing WDAT1 with RDAT1 in addition to the comparator 136 for comparing WDAT0 with RDAT0. A logical gate 136" may combine the signal $\Delta D0$ with a corresponding signal $\Delta D1$ that indicates whether there is a difference between the signals

WDAT1 and RDAT1. In response the logical gate 136" provides a signal ΔD which indicates whether at least one of the signals $\Delta D0$ or $\Delta D1$ indicates a difference, so as to enable the wait element 137 to pass on an active transition in the control signal provided by the repeater 34.

5 A further embodiment is shown in Figure 3. Parts therein corresponding to those of Figure 1 have reference number that is 200 higher. In the embodiment of Figure 3 both the first 210 and the second circuit module 220 operate synchronously, but they have independent clocks (Wclk, Rclk resp.). The selected one of the timing signals which controls the edge sensitive element 235 is the clock signal Wclk from the first circuit module 210. The 10 circuit includes an additional register 231A for transferring data from the transfer register 231 to the second circuit module 220. The control circuit comprises a comparable control chain for generating a control signal CRA for the auxiliary transfer register 231A. In particular the circuit includes a further edge sensitive element 235A for delaying an active transition in a control signal CRA for the auxiliary register 231A until a synchronizing transition is detected 15 in a timing signal Rclk from the second circuit module 220. The control chains for the transfer register 231 and the auxiliary transfer register 231A are mutually coupled via the shared arbitration element 238. The arbitration element 238 prevents that the transfer register 231 and the auxiliary transfer register 231A are updated at the same time.

Figure 4 shows a simplified embodiment having the same functionality as the 20 embodiment of Figure 3. Elements comparable to those of Figure 3 have a reference number which is 100 higher.

As in the embodiment of Figure 3 the synchronization module 330 comprises an auxiliary transfer register 331A. Here the control chain for both transfer register 331 and auxiliary transfer register 331A are mutually coupled via a sequencer 339, so as to form a 25 single chain. In this embodiment the further edge sensitive element 335A is part of the control chain.

In the embodiment the control signal CR for the transfer registers 331 and 331A repetitively undergoes the following stages. The first stage CR1 of the control signal is 30 generation of active events by the repeater 334. The repeater sends an event to the sequencer 339, which will then send this event to wait element 337 via signal CR2. In the next stage CR2 the active events are passed to the wait element 337 to be forwarded as stage 3 signal CR3 to the edge sensitive element 335 as soon as a difference is detected between input and output of the transfer register 331. The edge sensitive element 335 transfers the active 35 transitions in the stage 3 signal to the stage 4 signal CR4 if a synchronizing edge is detected

in the clock signal Wclk. The stage 4 signal on its turn causes the transfer register 331 to accept the new data offered by the first module 310. The transfer register 331 acknowledges this by a stage 5 signal CR5, which usually will be an unconditionally delayed version of the stage 4 signal CR4. The sequencer 339 passes this signal as stage 6 signal CR6 to the 5 auxiliary edge sensitive element 335A which transmits this as stage 7 signal CR7 upon detection of a synchronization transition in the clock signal Rclk. The signal CR7 causes the auxiliary transfer register 331A to accept new data from the transfer register 331. It provides signal CR8 to indicate completion to the sequencer 339, which passes this signal to the repeater 334. The repeater 334 on its turn then generates in a next round the stage 1 of the 10 control signal CR1. In this embodiment sequencer 339 prevents that the transfer register 231 and the auxiliary transfer register 231A are updated at the same time.

Figure 5 shows again another embodiment. It comprises an auxiliary register 431B for transferring data from the first module 410 to the register 431. The selected timing signal is a clock signal Rclk from the second circuit module 420. The timing signal from the 15 first circuit module 410 is a write request signal Wreg.

The signal chain comprises the first channel of the arbitration element 438, between a first input **a** coupled to the edge sensitive element 435 and a first output **b** coupled to a control input of the register 431. The register 431 has a control output coupled to repeater 434. The control input and the control output of register 431 are usually directly connected or 20 may alternatively be coupled via a delay function. The repeater 434 is coupled via wait element 437 to a first input **a** of the edge sensitive element 435. The second channel of the arbitration element 438 has a second input **c** for receiving the write request signal Wreq and a second output **d** for providing a control signal to control the auxiliary register 431B. The auxiliary register 431B may optionally include a delay element to provide a write 25 acknowledge signal Wack to the first circuit module 410 in response to the control signal Wreq. Alternatively the write acknowledge signal Wack may be provided without delay to the first circuit module 410.

The embodiments of figures 3, 4 and 5 can also be implemented without wait elements at the cost of additional power consumption.

30 Several circuits can be found in "Handshake Circuits: an Asynchronous Architecture for {VLSI} Programming" by "Kees van Berk, series = "International Series on Parallel Computation", volume 5, "Cambridge University Press", 1993, pp. 162-163. The article "Bridging Clock Domains by Synchronizing the Mice in the Mousetrap" by Joep Kessels and Ad Peeters and Suk-Jin Kim, editor: Jorge Juan Chico and Enrico Macii, Patmos

Incs, volume 2799, pp. "141--150", sep, 2003 describes several examples of synchronizing circuits. Also modules for conversion between two-phase and four-phase handshake signaling are well known to persons skilled in the art of asynchronous circuit design. The active clock edge, the passive clock edge or both can function as synchronization events in 5 signal St1 depending on the data valid requirements.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in a claim. The word 'a(n)' preceding an element does not 10 exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed general purpose processor. The invention resides in each new feature or combination of features.